What is claimed is:

1. A high speed semi-dynamic flip-flop circuit comprising:

a first supply voltage;

a second supply voltage;

a first clock signal;

a high-speed semi-dynamic flip-flop circuit first node;

a high-speed semi-dynamic flip-flop circuit OUT terminal;

a high-speed semi-dynamic flip-flop circuit data input terminal;

a high-speed semi-dynamic flip-flop circuit qbar out terminal;

a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode, said first supply voltage being coupled to said first transistor first flow electrode, said first clock signal being coupled to said first transistor control electrode, said first transistor second flow electrode being coupled to said high speed semi-dynamic flip-flop circuit first node;

a second transistor, said second transistor comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode, said first supply voltage being coupled to said second transistor first flow electrode, said second transistor second flow electrode being coupled to said high speed semi-dynamic flip-flop circuit first node;

a third transistor, said third transistor comprising a third transistor first flow electrode, a third transistor second flow electrode and a third

transistor control electrode, said first supply voltage being coupled to said third transistor first flow electrode, said third transistor control electrode being coupled to said high speed semi-dynamic flip-flop circuit first node, said third transistor second flow electrode being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal;

a delay circuit, comprising a delay circuit input and a delay circuit output, said delay circuit input being coupled to said first clock signal;

a NAND gate, said NAND gate comprising a NAND gate first input, a NAND gate second input, and a NAND gate output, said NAND gate first input being coupled to said delay circuit output, said NAND gate second input being coupled to said high speed semi-dynamic flip-flop circuit first node, said NAND gate output being coupled to said second transistor control electrode;

a fourth transistor, said fourth transistor comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode, said fourth transistor first flow electrode being coupled to said high speed semi-dynamic flip-flop circuit first node, said fourth transistor control electrode being coupled to said NAND gate output;

a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode, said fifth transistor first flow electrode being coupled to said fourth transistor second flow electrode, said fifth transistor control electrode being coupled to said high speed semi-dynamic flip-flop circuit data input terminal;

a sixth transistor, said sixth transistor comprising a sixth transistor first flow electrode, a sixth transistor second flow electrode and a sixth transistor control electrode, said sixth transistor

first flow electrode being coupled to said fifth transistor second flow electrode, said sixth transistor control electrode being coupled to said first clock signal, said sixth transistor second flow electrode being coupled to said second supply voltage;

a seventh transistor, said seventh transistor comprising a seventh transistor first flow electrode, a seventh transistor second flow electrode and a seventh transistor control electrode, said seventh transistor first flow electrode being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal, said seventh transistor control electrode control being coupled to said first clock signal;

an eighth transistor, said eighth transistor comprising a eighth transistor first flow electrode, a eighth transistor second flow electrode and a eighth transistor control electrode, said eighth transistor first flow electrode being coupled to said seventh transistor second flow electrode, said eighth transistor control electrode being coupled to said high speed semi-dynamic flip-flop circuit first node, said eighth transistor second flow electrode being coupled to said second supply voltage;

a third inverter, said third inverter comprising a third inverter input and a third inverter output, said third inverter input being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal, said third inverter output being coupled to said high speed semi-dynamic flip-flop circuit qbar out terminal;

a fourth inverter, said fourth inverter comprising a fourth inverter input and a fourth inverter output, said fourth inverter input being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal; and

a fifth inverter, said fifth inverter comprising a fifth inverter input and a fifth inverter output, said fifth inverter input being coupled to said fourth inverter output, said fifth inverter output being

coupled to said high speed semi-dynamic flip-flop circuit OUT terminal.

2. The high speed semi-dynamic flip-flop circuit of Claim 1, wherein,

said delay circuit comprises:

a first inverter, said first inverter comprising a first inverter input and a first inverter output, said first inverter input being coupled to said delay circuit input;

a second inverter, said second inverter comprising a second inverter input and a second inverter output, said second inverter input being coupled to said first inverter output, said second inverter output being coupled to said delay circuit output;

3. The high speed semi-dynamic flip-flop circuit of Claim 2, wherein,

Said first supply voltage is Vdd and said second supply voltage is ground.

4. The high speed semi-dynamic flip-flop circuit of Claim 3, wherein,

said first, second and third transistors are PFET transistors.

5. The high speed semi-dynamic flip-flop circuit of Claim 3, wherein,

said fourth, fifth, sixth, seventh and eighth transistors are NFET transistors.

6. A high speed semi-dynamic flip-flop circuit comprising:

a first supply voltage, Vdd;

a second supply voltage, ground;

a first clock signal;

a high-speed semi-dynamic flip-flop circuit first node;

a high-speed semi-dynamic flip-flop circuit OUT terminal;

a high-speed semi-dynamic flip-flop circuit data input terminal;

a high-speed semi-dynamic flip-flop circuit qbar out terminal;

a first transistor, said first transistor being a PFET transistor and comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode, said first supply voltage being coupled to said first transistor first flow electrode, said first clock signal being coupled to said first transistor control electrode, said first transistor second flow electrode being coupled to said high speed semi-dynamic flip-flop circuit first node;

a second transistor, said second transistor being a PFET transistor and comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode, said first supply voltage being coupled to said second transistor first flow electrode, said second transistor second flow electrode being coupled to said high speed semi-dynamic flip-flop circuit first node;

a third transistor, said third transistor being a PFET transistor and comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode, said first supply voltage being coupled to said third transistor first flow electrode, said third transistor

control electrode being coupled to said high speed semi-dynamic flip-flop circuit first node, said third transistor second flow electrode being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal;

a first inverter, said first inverter comprising a first inverter input and a first inverter output, said first inverter input being coupled to said first clock signal;

a second inverter, said second inverter comprising a second inverter input and a second inverter output, said second inverter input being coupled to said first inverter output;

a NAND gate, said NAND gate comprising a NAND gate first input, a NAND gate second input, and a NAND gate output, said NAND gate first input being coupled to said second inverter output, said NAND gate second input being coupled to said high speed semi-dynamic flip-flop circuit first node, said NAND gate output being coupled to said second transistor control electrode;

a fourth transistor, and said fourth transistor being a NFET transistor and comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode, said fourth transistor first flow electrode being coupled to said high speed semi-dynamic flip-flop circuit first node, said fourth transistor control electrode being coupled to said NAND gate output;

a fifth transistor, said fifth transistor being a NFET transistor and comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode, said fifth transistor first flow electrode being coupled to said fourth transistor second flow electrode, said fifth transistor control electrode being coupled to said high speed semi-dynamic flip-flop circuit data input terminal;;

a sixth transistor, said sixth transistor being a NFET transistor and comprising a sixth transistor first flow electrode, a sixth transistor second flow electrode and a sixth transistor control electrode, said sixth transistor first flow electrode being coupled to said fifth transistor second flow electrode, said sixth transistor control electrode being coupled to said first clock signal, said sixth transistor second flow electrode being coupled to said second supply voltage;

a seventh transistor, said seventh transistor being a NFET transistor and comprising a seventh transistor first flow electrode, a seventh transistor second flow electrode and a seventh transistor control electrode, said seventh transistor first flow electrode being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal, said seventh transistor control electrode control being coupled to said first clock signal;

an eighth transistor, said eighth transistor being a NFET transistor and comprising a eighth transistor first flow electrode, a eighth transistor second flow electrode and a eighth transistor control electrode, said eighth transistor first flow electrode being coupled to said seventh transistor second flow electrode, said eighth transistor control electrode being coupled to said high speed semi-dynamic flip-flop circuit first node, said eighth transistor second flow electrode being coupled to said second supply voltage;

a third inverter, said third inverter comprising a third inverter input and a third inverter output, said third inverter input being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal, said third inverter output being coupled to said high speed semi-dynamic flip-flop circuit qbar out terminal;

a fourth inverter, said fourth inverter comprising a fourth inverter input and a fourth inverter output,

said fourth inverter input being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal; and

a fifth inverter, said fifth inverter comprising a fifth inverter input and a fifth inverter output, said fifth inverter input being coupled to said fourth inverter output, said fifth inverter output being coupled to said high speed semi-dynamic flip-flop circuit OUT terminal.

7. A method for increasing the speed of semi-dynamic flip-flop circuits comprising:

supplying a first supply voltage;

supplying a second supply voltage;

supplying a first clock signal;

providing a high-speed semi-dynamic flip-flop circuit first node;

providing a high-speed semi-dynamic flip-flop circuit OUT terminal;

providing a high-speed semi-dynamic flip-flop circuit data input terminal;

providing a high-speed semi-dynamic flip-flop circuit qbar out terminal;

providing a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode;

coupling said first supply voltage to said first transistor first flow electrode;

coupling said first clock signal to said first transistor control electrode;

coupling said first transistor second flow electrode to said high-speed semi-dynamic flip-flop circuit first node;

providing a second transistor, said second transistor comprising a second transistor first flow

electrode, a second transistor second flow electrode and a second transistor control electrode;

coupling said first supply voltage to said second transistor first flow electrode;

coupling said second transistor second flow electrode to said high-speed semi-dynamic flip-flop circuit first node;

providing a third transistor, said third transistor comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode;

coupling said first supply voltage to said third transistor first flow electrode;

coupling said third transistor control electrode to said high-speed semi-dynamic flip-flop circuit first node;

coupling said third transistor second flow electrode to said high-speed semi-dynamic flip-flop circuit OUT terminal;

providing a delay circuit, comprising a delay circuit input and a delay circuit output;

coupling said delay circuit input to said first clock signal;

providing a NAND gate, said NAND gate comprising a NAND gate first input, a NAND gate second input, and a NAND gate output;

coupling said NAND gate first input to said delay circuit output;

coupling said NAND gate second input to said high-speed semi-dynamic flip-flop circuit first node;

coupling said NAND gate output to said second transistor control electrode;

providing a fourth transistor, said fourth transistor comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode;

coupling said fourth transistor first flow electrode to said high-speed semi-dynamic flip-flop circuit first node;

coupling said fourth transistor control electrode to said NAND gate output;

providing a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode;

coupling said fifth transistor first flow electrode to said fourth transistor second flow electrode;

coupling said fifth transistor control electrode to said high speed semi-dynamic flip-flop circuit data input terminal;;

providing a sixth transistor, said sixth transistor comprising a sixth transistor first flow electrode, a sixth transistor second flow electrode and a sixth transistor control electrode;

coupling said sixth transistor first flow electrode to said fifth transistor second flow electrode;

coupling said sixth transistor control electrode to said first clock signal;

coupling said sixth transistor second flow electrode to said second supply voltage;

providing a seventh transistor, said seventh transistor comprising a seventh transistor first flow electrode, a seventh transistor second flow electrode and a seventh transistor control electrode;

coupling said seventh transistor first flow electrode to said high-speed semi-dynamic flip-flop circuit OUT terminal;

coupling said seventh transistor control electrode control to said first clock signal;

providing an eighth transistor, said eighth transistor comprising a eighth transistor first flow

electrode, a eighth transistor second flow electrode and a eighth transistor control electrode;

coupling said eighth transistor first flow electrode to said seventh transistor second flow electrode;

coupling said eighth transistor control electrode to said high-speed semi-dynamic flip-flop circuit first node;

coupling said eighth transistor second flow electrode being coupled to said second supply voltage;

providing a third inverter, said third inverter comprising a third inverter input and a third inverter output;

coupling said third inverter input to said high-speed semi-dynamic flip-flop circuit OUT terminal;

coupling said third inverter output to said high-speed semi-dynamic flip-flop circuit qbar out terminal;

providing a fourth inverter, said fourth inverter comprising a fourth inverter input and a fourth inverter output;

coupling said fourth inverter input to said high-speed semi-dynamic flip-flop circuit OUT terminal;

providing a fifth inverter, said fifth inverter comprising a fifth inverter input and a fifth inverter output;

coupling said fifth inverter input being to said fourth inverter output; and

coupling said fifth inverter output to said high-speed semi-dynamic flip-flop circuit OUT terminal.

8. The method for increasing the speed of semi-dynamic flip-flop circuits of Claim 7, wherein, said providing a delay circuit comprises:

providing a first inverter, said first inverter comprising a first inverter input and a first inverter output;

coupling said first inverter input to said first clock signal;

providing a second inverter, said second inverter comprising a second inverter input and a second inverter output;

coupling said second inverter input to said first inverter output;

9. The method for increasing the speed of semi-dynamic flip-flop circuits of Claim 8, wherein,

said first supply voltage is Vdd and said second supply voltage is ground.

10. The method for increasing the speed of semi-dynamic flip-flop circuits of Claim 9, wherein,

said first, second and third transistors are PFET transistors.

11. The method for increasing the speed of semi-dynamic flip-flop circuits of Claim 9, wherein,

said fourth, fifth, sixth, seventh and eighth transistors are NFET transistors.

12. A method for increasing the speed of semi-dynamic flip-flop circuits comprising:

supplying a first supply voltage;

supplying a second supply voltage;

supplying a first clock signal;

providing a high-speed semi-dynamic flip-flop circuit first node;

providing a high-speed semi-dynamic flip-flop circuit OUT terminal;

providing high-speed semi-dynamic flip-flop circuit data input terminal;

providing a high-speed semi-dynamic flip-flop circuit qbar out terminal;

providing a first transistor, said first transistor being a PFET transistor and comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode;

coupling said first supply voltage to said first transistor first flow electrode;

coupling said first clock signal to said first transistor control electrode;

coupling said first transistor second flow electrode to said high-speed semi-dynamic flip-flop circuit first node;

providing a second transistor, said second transistor being a PFET transistor and comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode;

coupling said first supply voltage to said second transistor first flow electrode;

coupling said second transistor second flow electrode to said high-speed semi-dynamic flip-flop circuit first node;

providing a third transistor, said third transistor being a PFET transistor and comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode;

coupling said first supply voltage to said third transistor first flow electrode;

coupling said third transistor control electrode to said high-speed semi-dynamic flip-flop circuit first node;

coupling said third transistor second flow electrode to said high-speed semi-dynamic flip-flop circuit OUT terminal;

providing a first inverter, said first inverter comprising a first inverter input and a first inverter output;

coupling said first inverter input to said first clock signal;

providing a second inverter, said second inverter comprising a second inverter input and a second inverter output;

coupling said second inverter input to said first inverter output;

providing a NAND gate, said NAND gate comprising a NAND gate first input, a NAND gate second input, and a NAND gate output;

coupling said NAND gate first input to said second inverter output;

coupling said NAND gate second input to said high-speed semi-dynamic flip-flop circuit first node;

coupling said NAND gate output to said second transistor control electrode;

providing a fourth transistor, said fourth transistor being a NFET transistor and comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode;

coupling said fourth transistor first flow electrode to said high-speed semi-dynamic flip-flop circuit first node;

coupling said fourth transistor control electrode to said NAND gate output;

providing a fifth transistor, said fifth transistor being a NFET transistor and comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode;

coupling said fifth transistor first flow electrode to said fourth transistor second flow electrode;

coupling said fifth transistor control electrode to said high speed semi-dynamic flip-flop circuit data input terminal;;

providing a sixth transistor, said sixth transistor being a NFET transistor and comprising a sixth transistor first flow electrode, a sixth transistor second flow electrode and a sixth transistor control electrode;

coupling said sixth transistor first flow electrode to said fifth transistor second flow electrode;

coupling said sixth transistor control electrode to said first clock signal;

coupling said sixth transistor second flow electrode to said second supply voltage;

providing a seventh transistor, said seventh transistor being a NFET transistor and comprising a seventh transistor first flow electrode, a seventh transistor second flow electrode and a seventh transistor control electrode;

coupling said seventh transistor first flow electrode to said high-speed semi-dynamic flip-flop circuit OUT terminal;

coupling said seventh transistor control electrode control to said first clock signal;

providing an eighth transistor, said eighth transistor being a NFET transistor and comprising a eighth transistor first flow electrode, a eighth transistor second flow electrode and a eighth transistor control electrode;

coupling said eighth transistor first flow electrode to said seventh transistor second flow electrode;

coupling said eighth transistor control electrode to said high-speed semi-dynamic flip-flop circuit first node;

coupling said eighth transistor second flow electrode being coupled to said second supply voltage;

providing a third inverter, said third inverter comprising a third inverter input and a third inverter output;

coupling said third inverter input to said high-speed semi-dynamic flip-flop circuit OUT terminal;

coupling said third inverter output to said high-speed semi-dynamic flip-flop circuit qbar out terminal;

providing a fourth inverter, said fourth inverter comprising a fourth inverter input and a fourth inverter output;

coupling said fourth inverter input to said high-speed semi-dynamic flip-flop circuit OUT terminal;

providing a fifth inverter, said fifth inverter comprising a fifth inverter input and a fifth inverter output;

coupling said fifth inverter input being to said fourth inverter output; and

coupling said fifth inverter output to said high-speed semi-dynamic flip-flop circuit OUT terminal.